Abstract of the Disclosure

A synchronous mirror delay (SMD) clock recovery and skew adjustment circuit for an integrated circuit is described, having a reduced circuit implementation. The SMD clock recovery and skew adjustment circuit incorporates a delay segment into the forward delay line (FDL) and backward delay line (BDL) that accounts for all or some of the non-variable portion of the asserted clock signal time period. This delay segment allows reduction of the FDL and BDL lines to only those portions necessary to sense and adjust for the portion of the asserted clock signal time period that is variable and that must be adjusted for. The invention allows SMD clock recovery and skew adjustment circuits to be implemented in an optimized manner that exhibits a reduced overall circuit size.